

FIG. 1

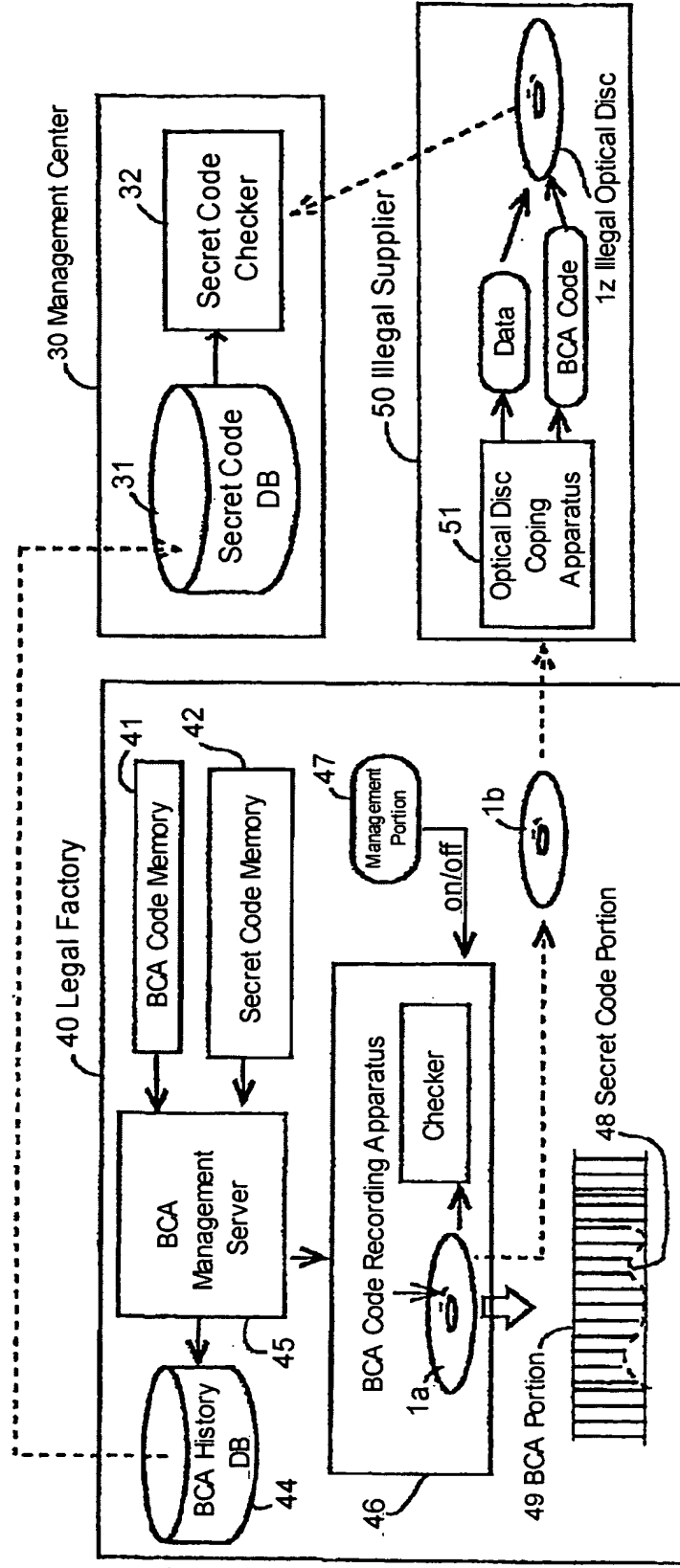


FIG. 2 (a)

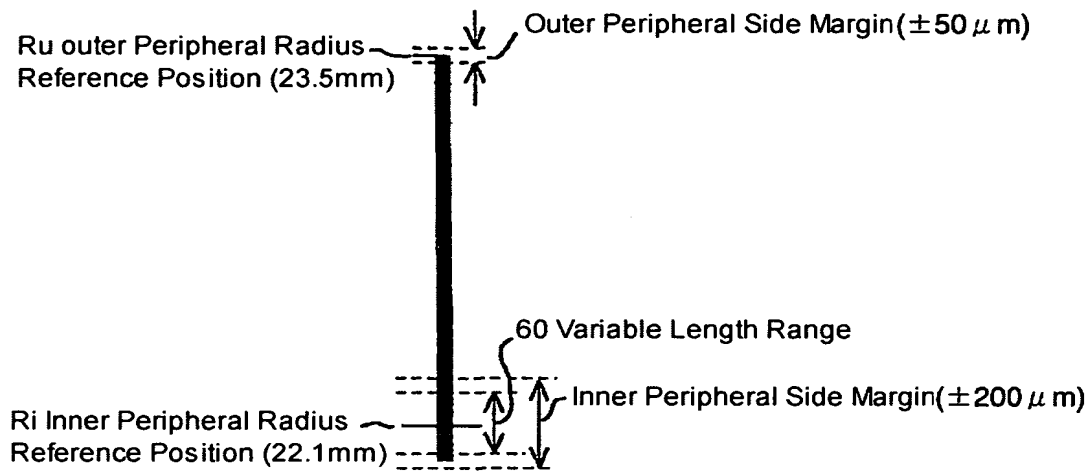


FIG. 2 (b)

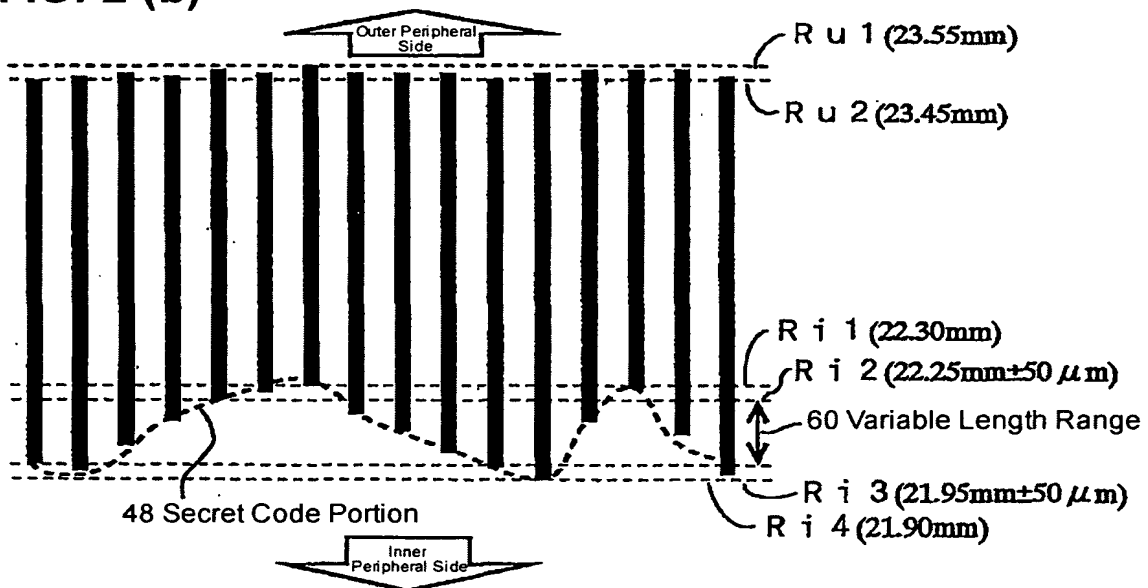


FIG. 3(a) M1 Standard of Mark Width ($10 \pm 5 \mu\text{m}$)

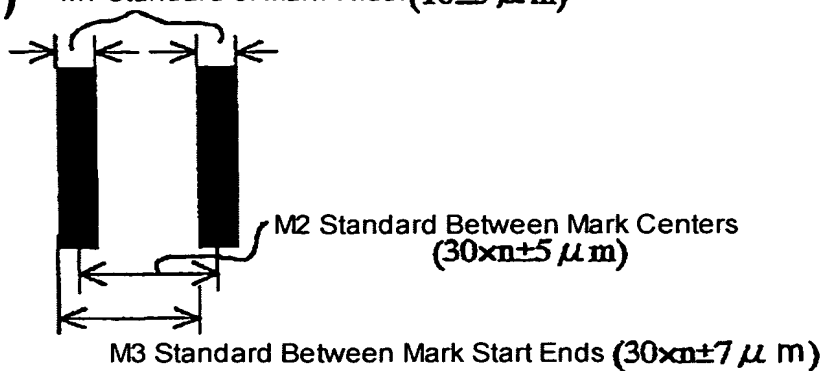


FIG. 3(b)

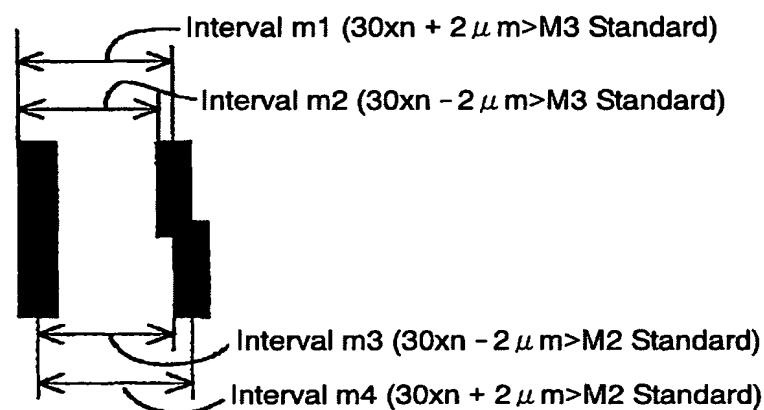


FIG. 3(c)

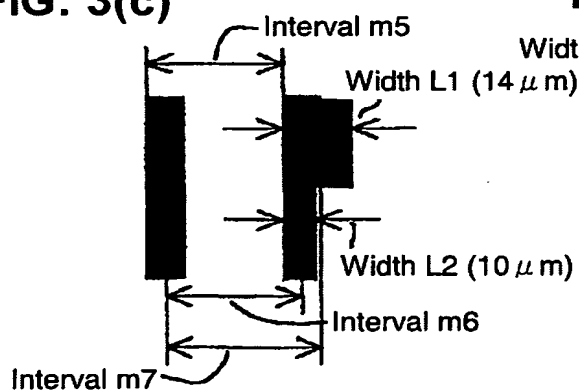


FIG. 3(d)

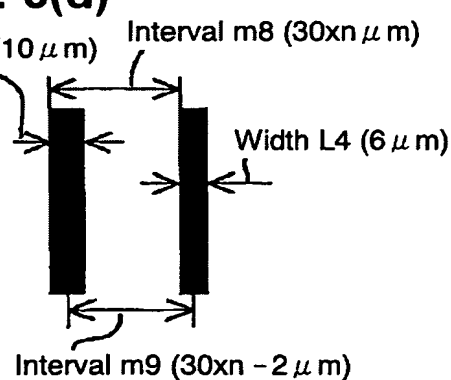


FIG. 4

The diagram illustrates the system architecture. At the top, a **60 Hoist Controller** is connected to a **19 Data Interface Portion**, which in turn connects to a central **14 Microprocessor**. The microprocessor is linked to several internal modules: **15 Secret Data Generation Portion**, **16 BCA Data Generation Portion**, **17 Data Buffer Portion**, **12 Focus Control Portion**, **13 Laser Output Control Portion**, and **18 Secret Data Superposition Portion**. It also receives feedback from **62 Clock Generation Portion** and **11 Carriage Control Portion**. The microprocessor controls the **7 Carriage** via the **11 Carriage Control Portion**, which is driven by a **4 Carriage Motor**. The carriage moves along a **5 Linear Scale** and is supported by a **6 Base**. The **7 Carriage** holds the **8 Optical Head**, which includes a **3 Laser Spot** and a **1 Disc Medium**. The optical head is also controlled by the **12 Focus Control Portion** and **13 Laser Output Control Portion**. The **8 Optical Head** is connected to a **2 Spindle Motor**, which is controlled by the **10 Spindle Control Portion** and provides input to the **62 Clock Generation Portion**. A **2a Rotary Encoder** is also connected to the spindle motor assembly.

FIG. 5

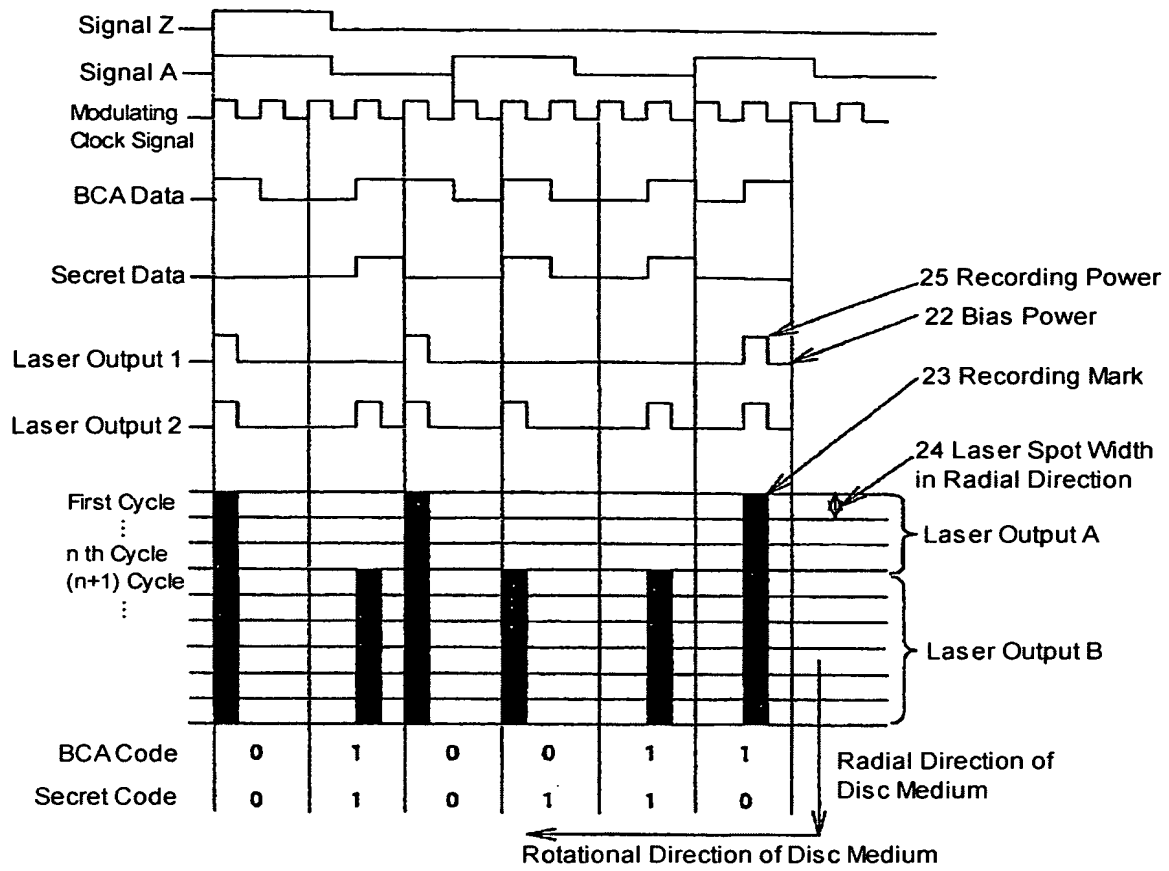


FIG. 6

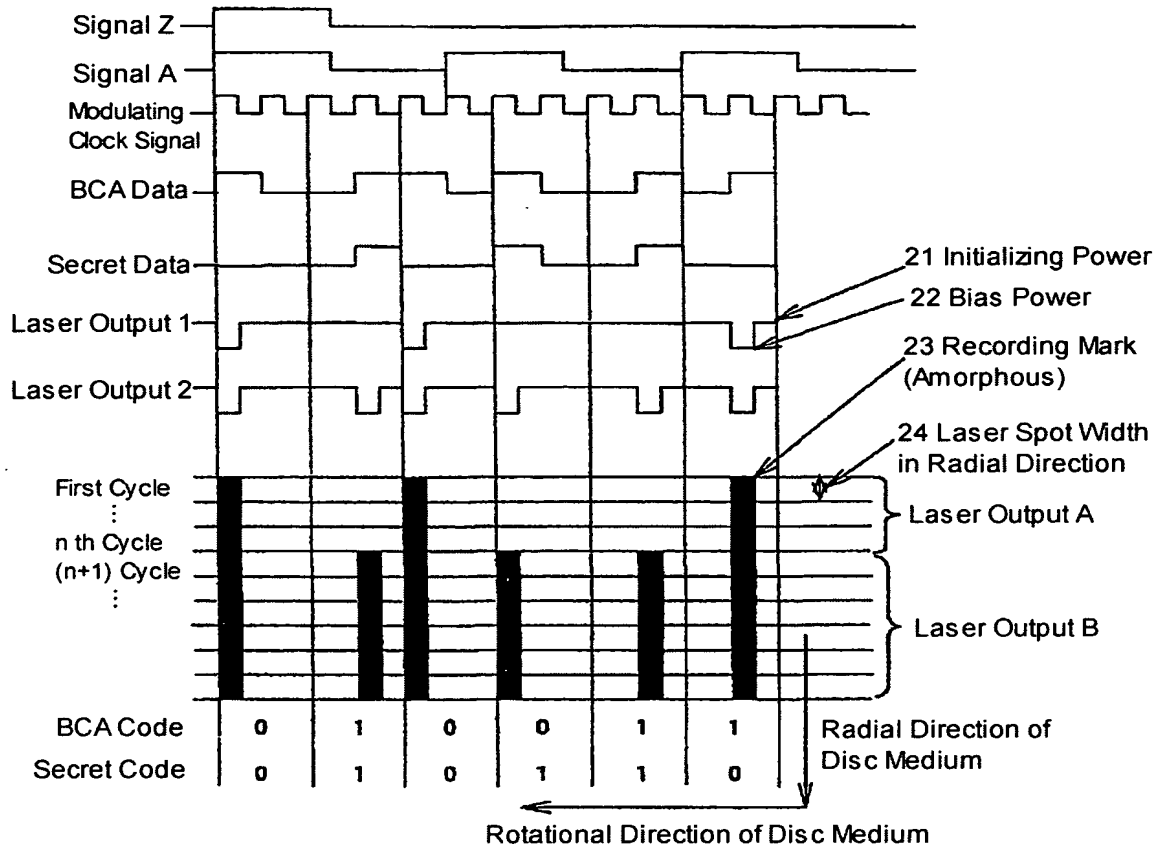
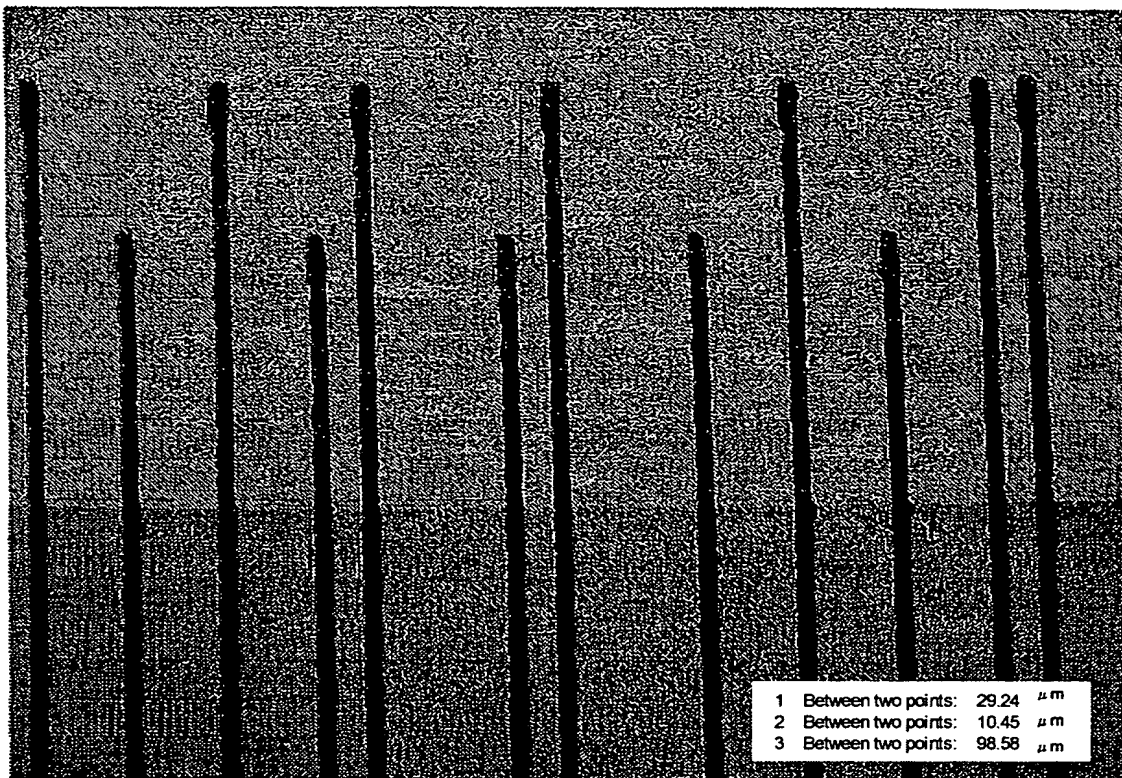


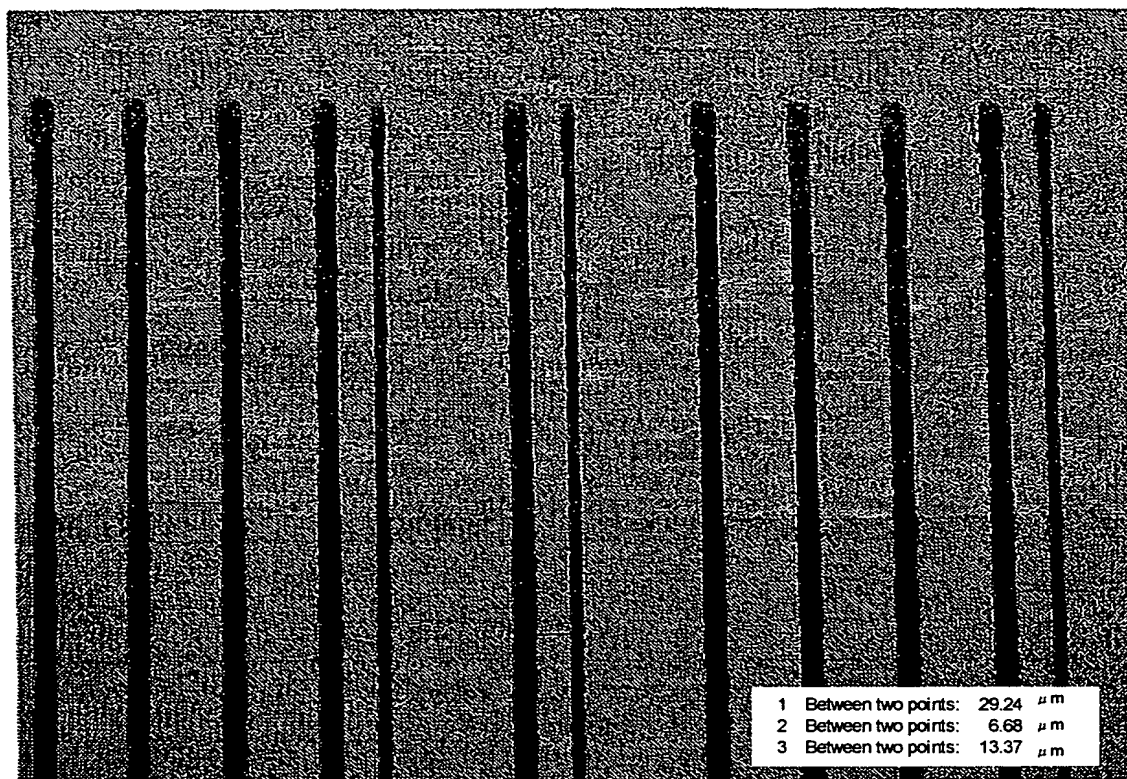
FIG. 7



BEST AVAILABLE COPY

BEST AVAILABLE COPY

FIG. 8



BEST AVAILABLE COPY